BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

PAT-NO: JP407093505A

DOCUMENT-IDENTIFIER: JP 07093505 A

TITLE: COUNT INTEGRATING DEVICE

PUBN-DATE: April 7, 1995

INVENTOR-INFORMATION:
NAME
HAYASHI, ZENRAI
NISHIMURA, MICHIAKI
KATO, SHINJI

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SHARP CORP	N/A

APPL-NO: JP05234533

APPL-DATE: September 21, 1993

INT-CL (IPC): G06M003/00, G03G021/02 , B41J029/20

ABSTRACT:

PURPOSE: To improve the reliability of important data inside ROMs and to reproduce the data even when a fault is generated by writing a total counter number and a checksum in the plural ROMs, comparing and confirming the data of the respective ROMs and then defining them as the accurate data.

CONSTITUTION: Registers A3, B4, C5 and D6 for tentatively storing the data and the checksum read from a storage memory 1 and the storage memory 2 and comparing and judging parts 7, 8 and 9 for checking and comparing the data of

the respective registers are provided inside a CPU 11. The total counter data
of the register A3 and the checksum of the register B4 are checked in the
comparing and judging part 7, the total counter data of the register C5 and the
checksum of the register D6 are checked in the comparing and judging part 8 and
the data of the registers A3 and C5 are compared in the comparing and judging
part 9. Then, when an errors is judged in the comparing and judging parts 7, 8
and 9, a user is informed of the error by a trouble display part 10.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 07-093505

(43)Date of publication of application : 07.04.1995

(51)Int.Cl. G06M 3/00
G03G 21/02
// B41J 29/20

(21)Application number : 05-234533

(22)Date of filing : 21.09.1993

(71)Applicant : SHARP CORP

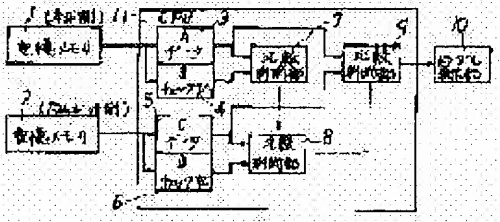
(72)Inventor : HAYASHI ZENRAI
NISHIMURA MICHIAKI
KATO SHINJI

(54) COUNT INTEGRATING DEVICE

(57)Abstract:

PURPOSE: To improve the reliability of important data inside ROMs and to reproduce the data even when a fault is generated by writing a total counter number and a checksum in the plural ROMs, comparing and confirming the data of the respective ROMs and then defining them as the accurate data.

CONSTITUTION: Registers A3, B4, C5 and D6 for tentatively storing the data and the checksum read from a storage memory 1 and the storage memory 2 and comparing and judging parts 7, 8 and 9 for checking and comparing the data of the respective registers are provided inside a CPU 11. The total counter data of the register A3 and the checksum of the register B4 are checked in the comparing and judging part 7, the total counter data of the register C5 and the checksum of the register D6 are checked in the comparing and judging part 8 and the data of the registers A3 and C5 are compared in the comparing and judging part 9. Then, when an errors is judged in the comparing and judging parts 7, 8 and 9, a user is informed of the error by a trouble display part 10.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] counting characterized by providing the following -- a means -- this -- counting -- counting which memorizes the data of the number of total counters by which counting was carried out with the means and which has two or more rewritable ROMs electrically -- addition equipment The means which writes said number of total counters and checksum in said two or more ROMs The means which reads these ****** rare ** data A means to compare the data of each of this ROM by which reading appearance was carried out A means to check the checksum of each ROM when the data of each of said ROM differ, and the means which answers said check means and is written in said ROM by using right data as normal data
[Claim 2] counting -- a means -- this -- counting -- counting which memorizes the data of the number of total counters by which counting was carried out with a means and which has two or more rewritable ROMs electrically -- counting characterized by to have a means carry out a part of address space of two or more of said ROMs in common, and perform coincidence writing and coincidence read-out in addition equipment, a means compare these data by which reading appearance was carried out, and a means generate an error signal only when said data differ -- addition equipment.

[Translation done.]

* NOTICES *

EXAMPLE

[Example] Hereafter, a detail is explained based on the example of this invention shown in the drawing. In addition, of course, it is not that by which this invention is limited to these examples.
[0011] The block diagram of this invention is shown in drawing 1 . The storage memory 1 and the storage memory 2 are rewritable ROMs electrically. The storage memory 1 is in a body and the storage memory 2 is in a drum unit. In the CPU11 interior, it has register A3 which memorizes temporarily the data and the checksum which were read from the storage memory 1 and the storage memory 2, register B4, a register C5, and a register D6, and has the comparative judgment sections 7, 8, and 9 which check and compare the data of each of said register. In the comparative judgment section 7, the total count data of register A3 and the checksum of register B4 are checked. In the comparative judgment section 8, the checksum of the total count data of a register C5 and a register D6 is checked. The comparative judgment section 9 compares register A3 and the data of C5. Moreover, when judged as an error in said comparative judgment sections 7, 8, and 9, there is a trouble display 10 which tells a user about an error.

[0012] The flow chart of the processing at the time of the completion of a copy (S1) and the processing at the time of a power source ON (S2) is shown in drawing 2 . The checksum of a total counter is calculated by adding 1 to a total counter at the time of the completion of a copy (201) (702). For example, when the total counter value before the completion of a copy is 1233, a total counter value is set to 1234 at the time of completion, and a checksum is set to 10 (1+2+3+4=10) which **(ed) the number of each digits. Next, a total counter value and a checksum value are written in said storage memory 1 and the storage memory 2 (203,204). A total counter value and a checksum are read from the storage memory 1 at the time of a power source ON (205). The checksum of the read total counter value is calculated (206), and as compared with the read checksum (207), if the value is the same, the usual processing will be started. When values differ, it judges that data changed and a total counter value and a checksum are read from the storage memory 2 (208). (for example, when the total counter value was 1234 and the checksum which the checksum was set to 10 (1+2+3+4), and was read is not 10) The checksum of the read total counter value is calculated (209), and is compared with the read checksum (210). If the value is the same, the data of the storage memory 2 will judge it as the right, and will go the data of the storage memory 2 into the storage memory 1 at writing (211) and the usual processing. When values differ, the total counter value read from the storage memory 1 and 2 is compared (212), and if the value is the same, it will judge that only the checksum value changed, a checksum will be calculated, and it will go into the repair storage memory 1 and 2 at writing (213) and the usual processing. When values differ, a memory trouble is displayed (214), and a machine is suspended. the above -- as an example 1 -- counting according to claim 1 -- the example of addition equipment was explained.
[0013] next -- as an example 2 -- counting according to claim 2 -- the example of addition equipment is explained. A block diagram is shown in drawing 3 . It has CPU32 and the storage memory 35 which control each I/O and memory in a body 31, and has the storage memory 36 in the drum unit 37. The storage memory 35 and 36 is rewritable ROM electrically. When it has the data select circuit 33 which can choose to which ROM the select signal from CPU performs the data writing and read-out in CPU

and storage memory and the data of ROM in which both electric rewritings are possible are not in agreement at the time of data readout, it has the data comparator circuit 34 which generates an error signal to CPU.

[0014] The configuration of CPU internal processing is shown in drawing 4 . 42 and 43 are the registers E and F which memorize temporarily the data read from enternal memory memory. A comparator 46 compares the checksum data memorized by this checksum value and register F43 in quest of the checksum value of the total count data memorized by the register E42. For example, if there is the interior of a register E42 by 1234, a checksum will be set to 10 (1+2+3+4=10), and a register F43 will compare whether it is 10. In the error signal check section 45, it is confirmed whether the error signal occurred from the external data comparator circuit. In the memory selection section 44, a memory selection signal is outputted [whether the data of the storage memory 1 or the storage memory 2 are inputted] for a command to the receptacle exterior from the decision section 47. In the decision section 47, it judges from which memory it reads next whether is a signal received from a comparator 46 and the error signal check section 45, and abnormalities are in data. In the decision section 48, it judges whether it indicates by the trouble. In the trouble display 49, a command is received from the decision section 48 and a memory trouble is displayed.

[0015] The flow chart of (S4) is shown in drawing 5 at the time of data readout at the time of data writing (S3). S3 is performed at the time of the completion of a copy, and S4 is performed at the time of a power source ON. It asks for a checksum from a total counter value at the time of data writing (501). Both the memory of the storage memory 1 and 2 is chosen (502), and a total counter value and a checksum are written in both memory (503). The storage memory 1 is chosen at the time of data readout (504), and a total counter value and a checksum are read to the register in CPU (505). It is confirmed whether the error signal occurred from the data comparator circuit at the time of read-out (506). If there is no error signal, processing will usually be started. If it is, a checksum will be calculated from the read total counter value, and this checksum will be compared with the read checksum (507). If the same, processing will usually be started. If it differs, the storage memory 2 will be chosen (508), and a total counter value and a checksum are read to the register in CPU (509). It processes like the above (510). If the same, the total counter value and checksum which were read from the storage memory 2 to the storage memory 1 will be written in (511), and processing will usually be started. When it differs, it judges that memory is unusual and a memory trouble is displayed (512), and a machine is suspended.

[0016] In addition, as for this invention, it is needless to say that it deforms suitably and can carry out within limits which are not limited only to the example which described above and was shown in the drawing, and do not deviate from a summary.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the important section block diagram of this invention equipment.
[Drawing 2] It is the flow chart which shows actuation of this invention.
[Drawing 3] It is the block diagram of this invention equipment.
[Drawing 4] It is a block diagram in CPU of this invention equipment.
[Drawing 5] It is the flow chart which shows actuation of this invention.
[Drawing 6] It is the important section block diagram of equipment conventionally.
[Drawing 7] It is the flow chart which shows actuation of equipment conventionally.
[Description of Notations]
1 Storage Memory (Body Side)
2 Storage Memory (Drum Unit Side)
3 Register A
4 Register B
5 Register C
6 Register D
7 Comparative Judgment Section
8 Comparative Judgment Section
9 Comparative Judgment Section
10 Trouble Display
11 CPU
31 Body
32 CPU
33 Data Select Circuit
34 Data Comparator Circuit
35 Storage Memory
36 Storage Memory
37 Drum Unit
41 CPU
42 Register E
43 Register F
44 Memory Selection Section
45 Error Signal Check Section
46 Comparator
47 Decision Section
48 Decision Section
49 Trouble Display
61 CPU
62 ROM

[Translation done.]

* NOTICES *

OPERATION

[Function] the above-mentioned configuration -- counting according to claim 1 -- according to addition equipment, it aims at the thing in a copying machine for which the dependability of important data, such as a total counter, is electrically raised using rewritable ROM, and the dependability of the important data in rewritable ROM improves electrically, without carrying out a cost rise by performing all by 1. software processing.
[0008] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained. counting according to claim 2 -- according to addition equipment, it aims at shortening the check time amount of data and raising the dependability of important data, such as a total counter, and the processing time can be shortened by performing check processing of 1. data in a data comparator circuit.
[0009] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] this invention -- counting -- it makes to addition equipment for the purpose of solution of the above-mentioned technical problem characterized by providing the following -- having -- counting according to claim 1 -- addition equipment -- counting -- a means -- this -- counting -- counting which memorizes the data of the number of total counters by which counting was carried out with the means and which has two or more rewritable ROMs electrically -- addition equipment. The means which writes said number of total counters and checksum in said two or more ROMs The means which reads these ****** rare ** data A means to compare the data of each of this ROM by which reading appearance was carried out A means to check the checksum of each ROM when the data of each of said ROM differ, and the means which answers said check means and is written in said ROM by using right data as normal data
[0006] In addition equipment counting according to claim 2 -- addition equipment -- counting -- a means -- this -- counting -- counting which memorizes the data of the number of total counters by which counting was carried out with the means and which has two or more rewritable ROMs electrically -- counting characterized by having a means to carry out a part of address space of two or more of said ROMs in common, and to perform coincidence writing and coincidence read-out, a means to compare these data by which reading appearance was carried out, and a means to generate an error signal only when said data differ -- it is addition equipment.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the case of the conventional technique, since the value and checksum which calculated the checksum of a total counter value were compared and it differed, although the display of a memory trouble is possible, since it becomes impossible to judge an exact total counter value at this time, the dependability of a total counter is required for the appearance which does not become a memory trouble. Moreover, with the conventional technique, since the total counter value and the checksum are memorized by one ROM, it can do only by raising the dependability of ROM for raising the dependability of a total counter.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] counting of this invention according to claim 1 -- according to addition equipment, it aims at the thing in a copying machine for which the dependability of important data, such as a total counter, is electrically raised using rewritable ROM, and the dependability of the important data in rewritable ROM improves electrically, without carrying out a cost rise by performing all by 1. software processing.
[0018] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained.
[0019] counting according to claim 2 -- according to addition equipment, it aims at shortening the check time amount of data and raising the dependability of important data, such as a total counter, and the processing time can be shortened by performing check processing of 1. data in a data comparator circuit.

[0020] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] It has rewritable ROM62 electrically with CPU61 which controls a load, a sensor, etc. as conventionally shown in a copy system at the block diagram of drawing 6 , and controls memory. The value which totaled the store circuit which memorizes the use count of a copying machine when it was called a total counter, for example, the time of energization and a power source were not electrically switched on by rewritable ROM is held.
[0003] The flows of control of a total counter are shown in drawing 7 . The checksum value of a total counter value is calculated by adding 1 to a total counter at the time of the completion of a copy (S5) (701) (702), and a total counter value and a checksum value are electrically written in rewritable ROM (703,704). The checksum of read-out (705) and the read total counter value is calculated for a power up (S6), a total counter value, and a checksum value (706), if the same, when it enters and differs in the usual processing as compared with the read checksum (707 708), a memory trouble is displayed (709), and a machine is suspended. By the object which a checksum value is a checksum value and confirms whether the total counter value is changing at the time of a power source OFF, the whole of each digit of a total counter value is added, and it asks. For example, it is set to 10 when a total counter value is 1234 (1+2+3+4=10). In addition, JP,62-27759,A is mentioned as well-known data of the above-mentioned contents of explanation.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] counting of the reproducing unit which this invention has rewritable ROM electrically in body control, and has the same ROM as the above in a drum unit, a development unit, etc. -- it is related with addition equipment.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] counting of the reproducing unit which this invention has rewritable ROM electrically in body control, and has the same ROM as the above in a drum unit, a development unit, etc. -- it is related with addition equipment.
[0002]
[Description of the Prior Art] It has rewritable ROM62 electrically with CPU61 which controls a load, a sensor, etc. as conventionally shown in a copy system at the block diagram of drawing 6 , and controls memory. The value which totaled the store circuit which memorizes the use count of a copying machine when it was called a total counter, for example, the time of energization and a power source were not electrically switched on by rewritable ROM is held.
[0003] The flows of control of a total counter are shown in drawing 7 . The checksum value of a total counter value is calculated by adding 1 to a total counter at the time of the completion of a copy (S5) (701) (702), and a total counter value and a checksum value are electrically written in rewritable ROM (703,704). The checksum of read-out (705) and the read total counter value is calculated for a power up (S6), a total counter value, and a checksum value (706), if the same, when it enters and differs in the usual processing as compared with the read checksum (707 708), a memory trouble is displayed (709), and a machine is suspended. By the object which a checksum value is a checksum value and confirms whether the total counter value is changing at the time of a power source OFF, the whole of each digit of a total counter value is added, and it asks. For example, it is set to 10 when a total counter value is 1234 (1+2+3+4=10). In addition, JP,62-27759,A is mentioned as well-known data of the above-mentioned contents of explanation.
[0004]
[Problem(s) to be Solved by the Invention] In the case of the conventional technique, since the value and checksum which calculated the checksum of a total counter value were compared and it differed, although the display of a memory trouble is possible, since it becomes impossible to judge an exact total counter value at this time, the dependability of a total counter is required for the appearance which does not become a memory trouble. Moreover, with the conventional technique, since the total counter value and the checksum are memorized by one ROM, it can do only by raising the dependability of ROM for raising the dependability of a total counter.
[0005]
[Means for Solving the Problem] this invention is made for the purpose of solution of the above-mentioned technical problem -- having -- counting according to claim 1 -- addition equipment In addition equipment counting -- a means -- this -- counting -- counting which memorizes the data of the number of total counters by which counting was carried out with the means and which has two or more rewritable ROMs electrically -- The means which writes said number of total counters and checksum in said two or more ROMs, The means which reads these ****** rare ** data, and a means to compare the data of each of this ROM by which reading appearance was carried out, counting characterized by

having a means to check the checksum of each ROM when the data of each of said ROM differ, and the means which answers said check means and is written in said ROM by using right data as normal data -- it is addition equipment.
[0006] In addition equipment counting according to claim 2 -- addition equipment -- counting -- a means -- this -- counting -- counting which memorizes the data of the number of total counters by which counting was carried out with the means and which has two or more rewritable ROMs electrically -- counting characterized by having a means to carry out a part of address space of two or more of said ROMs in common, and to perform coincidence writing and coincidence read-out, a means to compare these data by which reading appearance was carried out, and a means to generate an error signal only when said data differ -- it is addition equipment.
[0007]
[Function] the above-mentioned configuration -- counting according to claim 1 -- according to addition equipment, it aims at the thing in a copying machine for which the dependability of important data, such as a total counter, is electrically raised using rewritable ROM, and the dependability of the important data in rewritable ROM improves electrically, without carrying out a cost rise by performing all by 1. software processing.
[0008] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained. counting according to claim 2 -- according to addition equipment, it aims at shortening the check time amount of data and raising the dependability of important data, such as a total counter, and the processing time can be shortened by performing check processing of 1. data in a data comparator circuit.
[0009] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained.
[0010]
[Example] Hereafter, a detail is explained based on the example of this invention shown in the drawing. In addition, of course, it is not that by which this invention is limited to these examples.
[0011] The block diagram of this invention is shown in drawing 1 . The storage memory 1 and the storage memory 2 are rewritable ROMs electrically. The storage memory 1 is in a body and the storage memory 2 is in a drum unit. In the CPU11 interior, it has register A3 which memorizes temporarily the data and the checksum which were read from the storage memory 1 and the storage memory 2, register B4, a register C5, and a register D6, and has the comparative judgment sections 7, 8, and 9 which check and compare the data of each of said register. In the comparative judgment section 7, the total count data of register A3 and the checksum of register B4 are checked. In the comparative judgment section 8, the checksum of the total count data of a register C5 and a register D6 is checked. The comparative judgment section 9 compares register A3 and the data of C5. Moreover, when judged as an error in said comparative judgment sections 7, 8, and 9, there is a trouble display 10 which tells a user about an error.

[0012] The flow chart of the processing at the time of the completion of a copy (S1) and the processing at the time of a power source ON (S2) is shown in drawing 2 . The checksum of a total counter is calculated by adding 1 to a total counter at the time of the completion of a copy (201) (702). For example, when the total counter value before the completion of a copy is 1233, a total counter value is set to 1234 at the time of completion, and a checksum is set to 10 (1+2+3+4=10) which **(ed) the number of each digits. Next, a total counter value and a checksum value are written in said storage memory 1 and the storage memory 2 (203,204). A total counter value and a checksum are read from the storage memory 1 at the time of a power source ON (205). The checksum of the read total counter value is calculated (206), and as compared with the read checksum (207), if the value is the same, the usual processing will be started. When values differ, it judges that data changed and a total counter value and a checksum are read from the storage memory 2 (208). (for example, when the total counter value was 1234 and the checksum which the checksum was set to 10 (1+2+3+4), and was read is not 10) The checksum of the read total counter value is calculated (209), and is compared with the read checksum (210). If the value is the same, the data of the storage memory 2 will judge it as the right, and will go the

data of the storage memory 2 into the storage memory 1 at writing (211) and the usual processing. When values differ, the total counter value read from the storage memory 1 and 2 is compared (212), and if the value is the same, it will judge that only the checksum value changed, a checksum will be calculated, and it will go into the repair storage memory 1 and 2 at writing (213) and the usual processing. When values differ, a memory trouble is displayed (214), and a machine is suspended. the above -- as an example 1 -- counting according to claim 1 -- the example of addition equipment was explained.
[0013] next -- as an example 2 -- counting according to claim 2 -- the example of addition equipment is explained. A block diagram is shown in drawing 3 . It has CPU32 and the storage memory 35 which control each I/O and memory in a body 31, and has the storage memory 36 in the drum unit 37. The storage memory 35 and 36 is rewritable ROM electrically. When it has the data select circuit 33 which can choose to which ROM the select signal from CPU performs the data writing and read-out in CPU and storage memory and the data of ROM in which both electric rewritings are possible are not in agreement at the time of data readout, it has the data comparator circuit 34 which generates an error signal to CPU.
[0014] The configuration of CPU internal processing is shown in drawing 4 . 42 and 43 are the registers E and F which memorize temporarily the data read from enternal memory memory. A comparator 46 compares the checksum data memorized by this checksum value and register F43 in quest of the checksum value of the total count data memorized by the register E42. For example, if there is the interior of a register E42 by 1234, a checksum will be set to 10 (1+2+3+4=10), and a register F43 will compare whether it is 10. In the error signal check section 45, it is confirmed whether the error signal occurred from the external data comparator circuit. In the memory selection section 44, a memory selection signal is outputted [whether the data of the storage memory 1 or the storage memory 2 are inputted] for a command to the receptacle exterior from the decision section 47. In the decision section 47, it judges from which memory it reads next whether is a signal received from a comparator 46 and the error signal check section 45, and abnormalities are in data. In the decision section 48, it judges whether it indicates by the trouble. In the trouble display 49, a command is received from the decision section 48 and a memory trouble is displayed.
[0015] The flow chart of (S4) is shown in drawing 5 at the time of data readout at the time of data writing (S3). S3 is performed at the time of the completion of a copy, and S4 is performed at the time of a power source ON. It asks for a checksum from a total counter value at the time of data writing (501). Both the memory of the storage memory 1 and 2 is chosen (502), and a total counter value and a checksum are written in both memory (503). The storage memory 1 is chosen at the time of data readout (504), and a total counter value and a checksum are read to the register in CPU (505). It is confirmed whether the error signal occurred from the data comparator circuit at the time of read-out (506). If there is no error signal, processing will usually be started. If it is, a checksum will be calculated from the read total counter value, and this checksum will be compared with the read checksum (507). If the same, processing will usually be started. If it differs, the storage memory 2 will be chosen (508), and a total counter value and a checksum are read to the register in CPU (509). It processes like the above (510). If the same, the total counter value and CHI <DP N=0004> EKKUSAMU which were read from the storage memory 2 to the storage memory 1 will be written in (511), and processing will usually be started. When it differs, it judges that memory is unusual and a memory trouble is displayed (512), and a machine is suspended.
[0016] In addition, as for this invention, it is needless to say that it deforms suitably and can carry out within limits which are not limited only to the example which described above and was shown in the drawing, and do not deviate from a summary.
[0017]
[Effect of the Invention] counting of this invention according to claim 1 -- according to addition equipment, it aims at the thing in a copying machine for which the dependability of important data, such as a total counter, is electrically raised using rewritable ROM, and the dependability of the important data in rewritable ROM improves electrically, without carrying out a cost rise by performing all by 1. software processing.

[0018] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained.
[0019] counting according to claim 2 -- according to addition equipment, it aims at shortening the check time amount of data and raising the dependability of important data, such as a total counter, and the processing time can be shortened by performing check processing of 1. data in a data comparator circuit.

[0020] Since data are memorized to ROM of another side even if one side breaks down by [2.2] using rewritable ROM electrically, the return of data is attained.

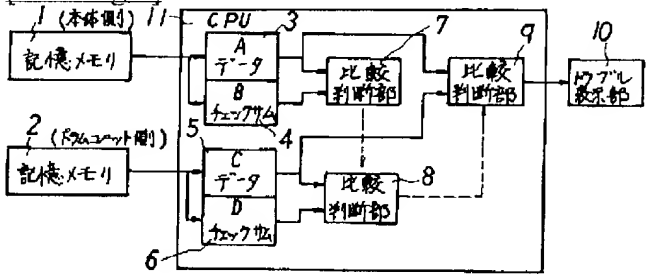
[Translation done.]

* NOTICES *

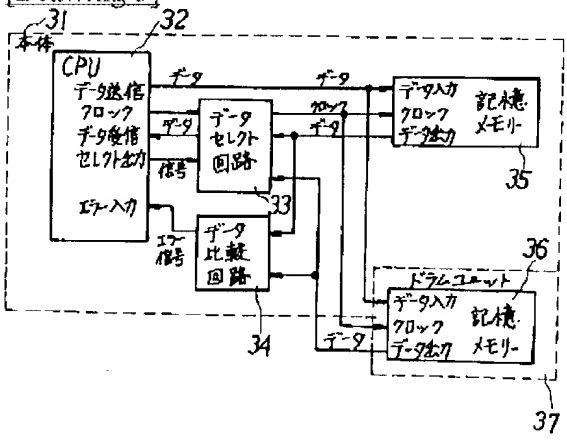
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

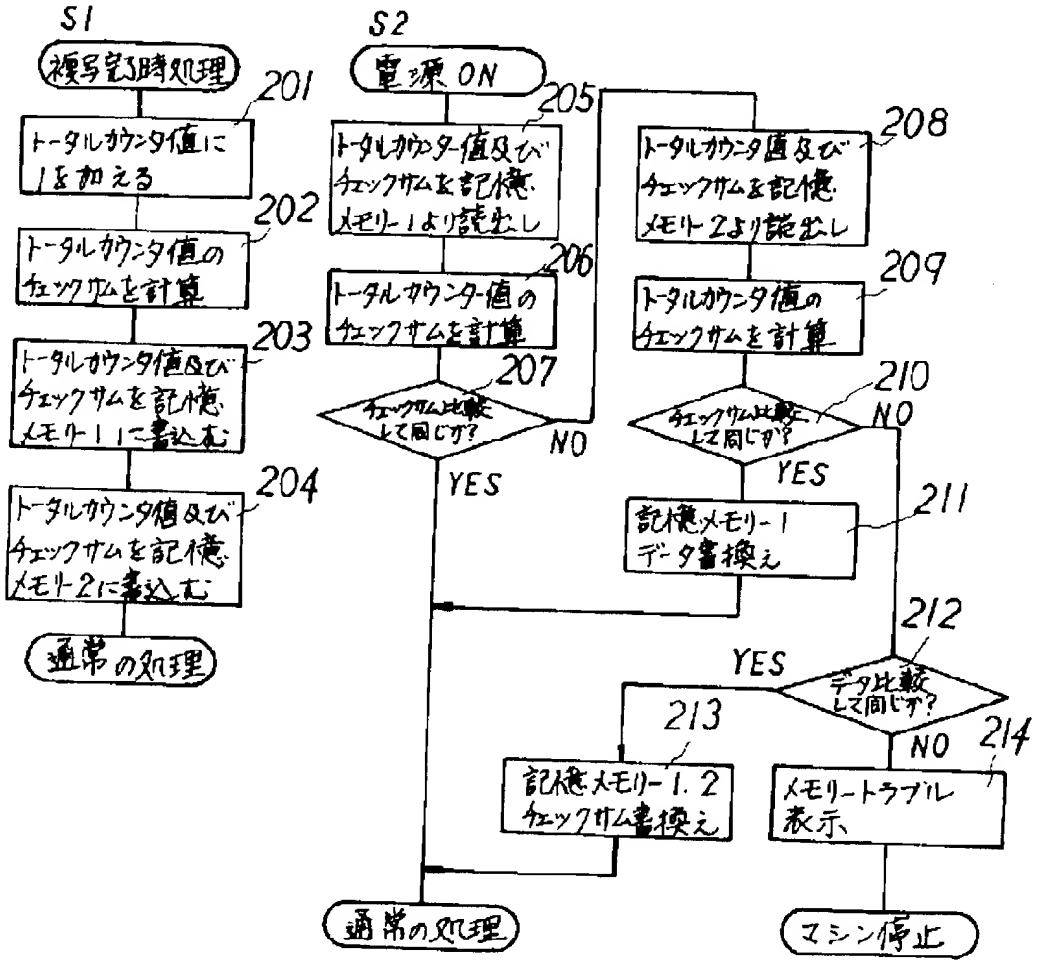
[Drawing 1]



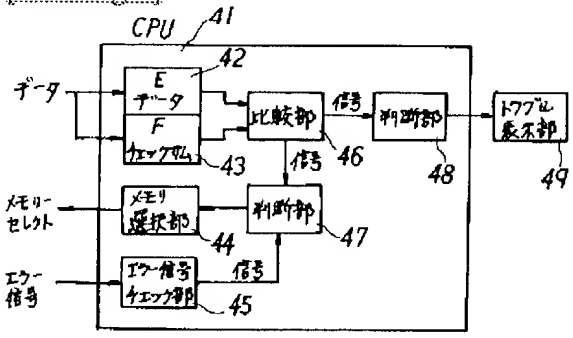
[Drawing 3]



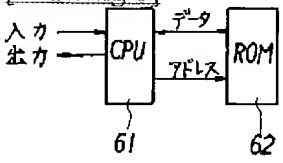
[Drawing 2]



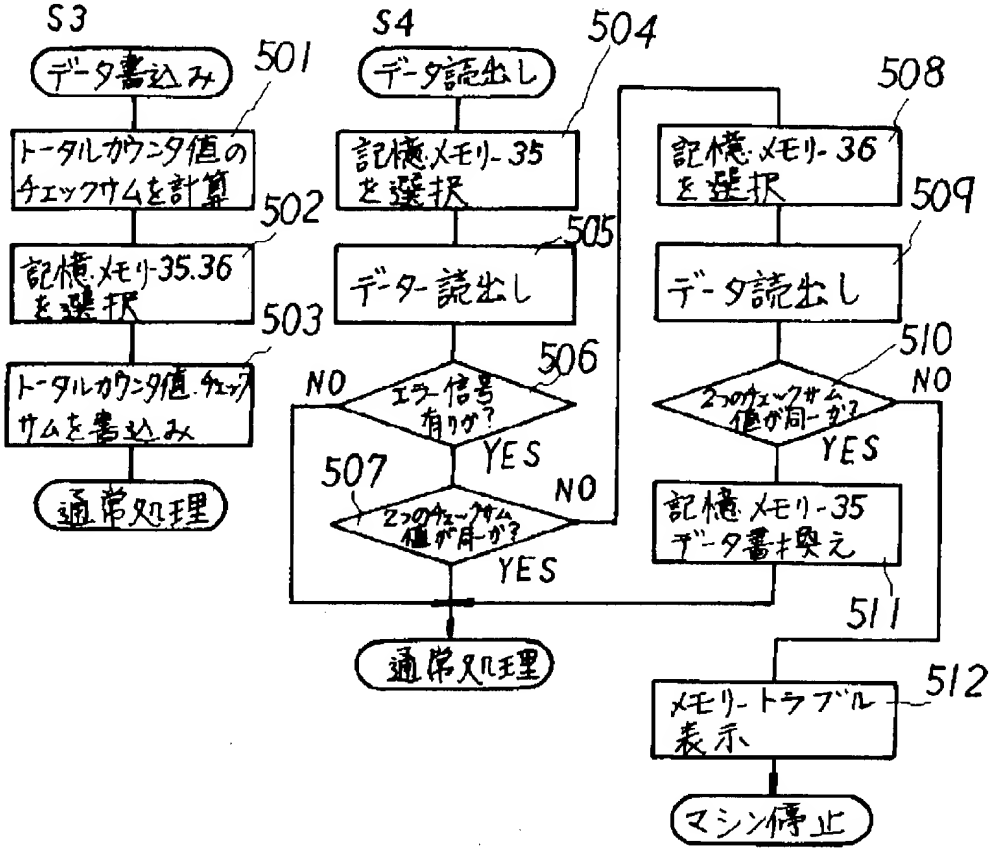
[Drawing 4]



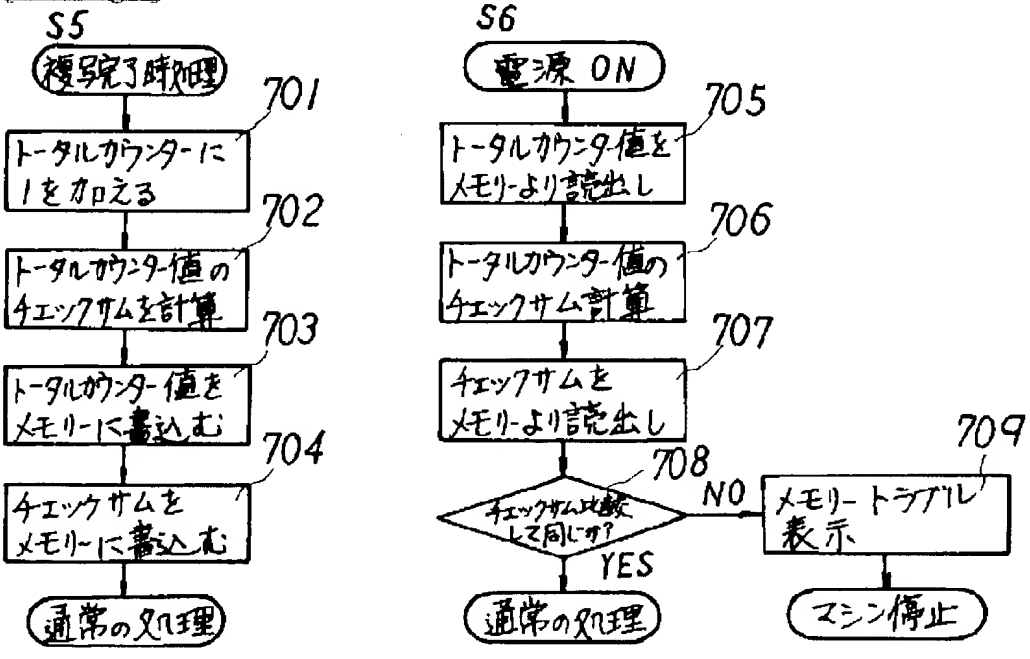
[Drawing 6]



[Drawing 5]



[Drawing 7]



[Translation done.]